

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L11	110	"N.sub.20" with "H.sub.2"	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 13:25
2	BRS	L12	73	11 and uniform\$3	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 13:52
3	BRS	L13	64	12 and nitrogen	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 13:56
4	BRS	L16	0	14 and 15	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 13:57
5	BRS	L17	36	13 and 14	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 13:57

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L14	57	"N.sub.20" adj3 "H.sub.2"	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 14:23
7	BRS	L18	53	14 and nitrogen	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 14:54
8	BRS	L19	0	15 and 18	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 14:54
9	BRS	L15	440	uniform\$3 adj3 nitrogen	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 16:10
10	IS&R	L20	166	(438/775).CCLS.	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 16:11

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	IS&R	L23	506	(438/787).CCLS.	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 16:58
12	IS&R	L24	266	(438/791).CCLS.	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2003/03/03 17:15

US-PAT-NO: 6235590

DOCUMENT-IDENTIFIER: US 6235590 B1

TITLE: Fabrication of differential gate oxide thicknesses
on a single
integrated circuit chip

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Various implementations include one or more of the following advantages. An integrated circuit having multiple gate oxides with different thicknesses can be fabricated. The different oxide thicknesses can be used, for example, in the fabrication of devices formed on a single wafer and requiring different operating voltages. Additionally, the invention allows gate oxides having different thicknesses and with a relatively high nitrogen content to be formed.

The high nitrogen content can help prevent the diffusion of boron ions from the gate electrodes into the oxynitride gates, thereby improving device characteristics. For example, the high nitrogen concentration can give the devices a higher voltage tolerance and make them more resistant to breakdown.

The device performance and lifetime of dual gate CMOS and circuits can, thereby be improved. Formation of the gate oxides in a high pressure furnace also can result in a more uniform distribution of nitrogen throughout the gate oxide which also improves performance of the devices.

Additionally, the foregoing technique allows gate oxides with a relatively high nitrogen content to be formed. The high nitrogen concentration can give the devices 12, 14 a higher voltage tolerance and make them more resistant to

breakdown. In particular, the high nitrogen content can reduce or prevent the diffusion of boron ions from the poly-Si gate electrodes 30 into the gate oxides 16, 18 during subsequent thermal annealing processes. The device performance and lifetime can, thereby be improved. Formation of the gate oxides 16, 18 in a high pressure furnace also can result in a more uniform distribution of nitrogen throughout the gate oxide which also improves performance of the devices.

US-PAT-NO: 5952771

DOCUMENT-IDENTIFIER: US 5952771 A

TITLE: Micropoint switch for use with field emission display and method for making same

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The second benefit achieved from annealing is the distribution of nitrogen within nitride oxidation layer 509 (FIG. 5D). Specifically, the high temperatures experienced in the steps of blocks 415 and 416 will anneal structure 526 resulting in a relatively uniform distribution of nitrogen throughout layer 509. Such distribution creates a more uniform V_{sub.t} for all MOSFETs on the subject wafer which, in turn, produces a relatively uniform screen brightness in FEDs (i.e., minimizes bright spots). This is a critical parameter for successful FED operation.